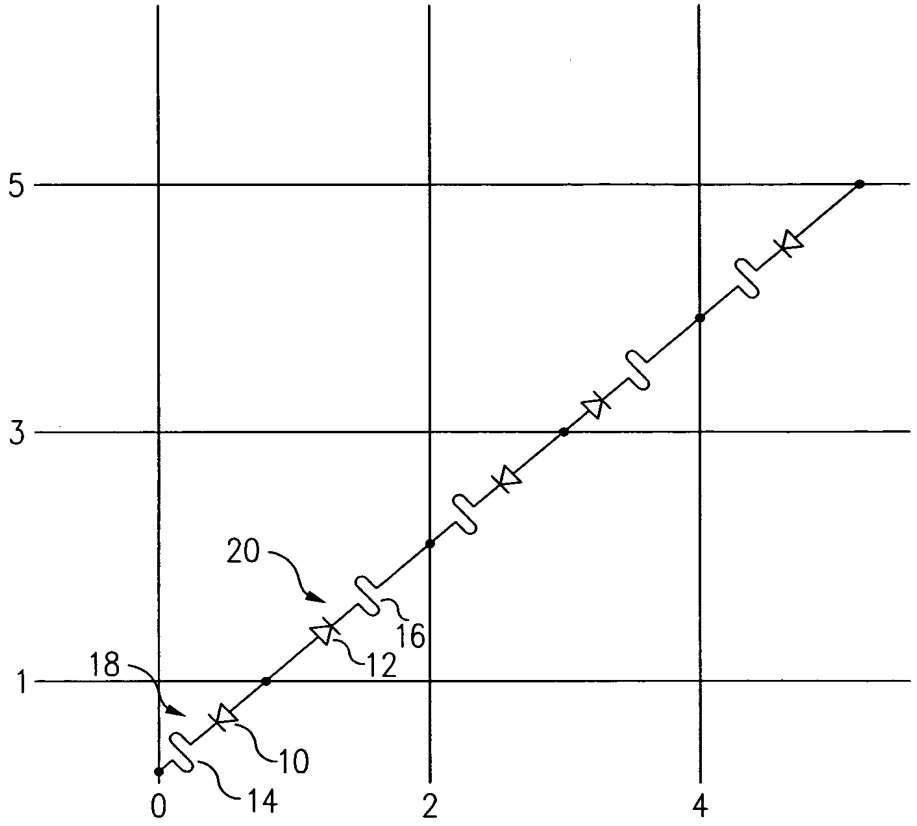

5
3
1
0
2
4
20
16
12
18
10
14

FIG. 1

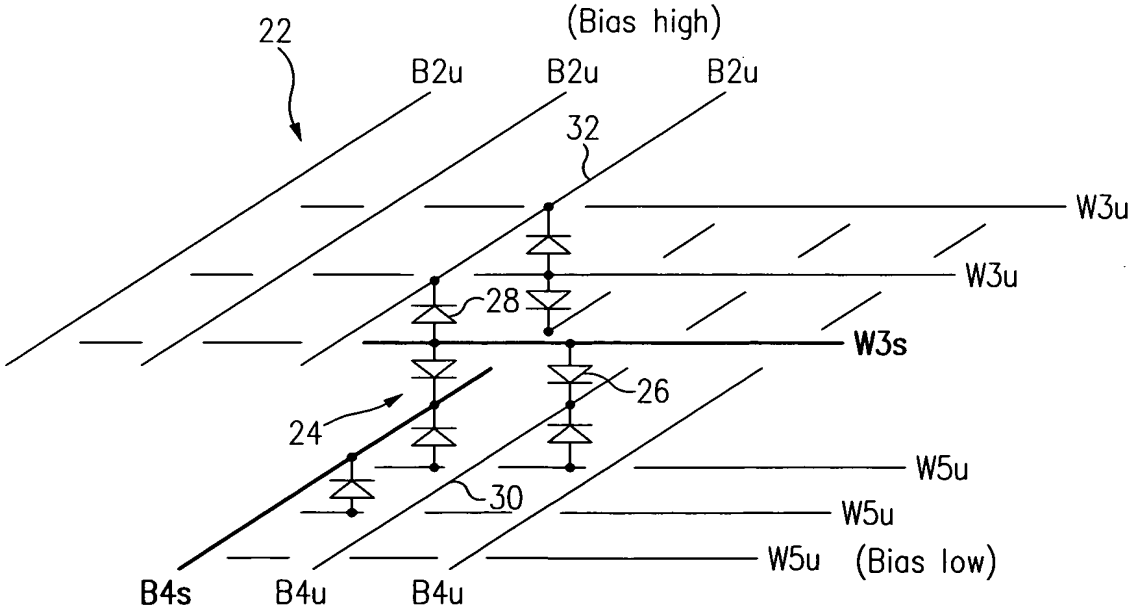

22
(Bias high)
B2u
B2u
B2u
32
W3u
W3u
28
W3s
26
24
W5u
30
W5u
W5u
(Bias low)
B4s
B4u
B4u

FIG. 2

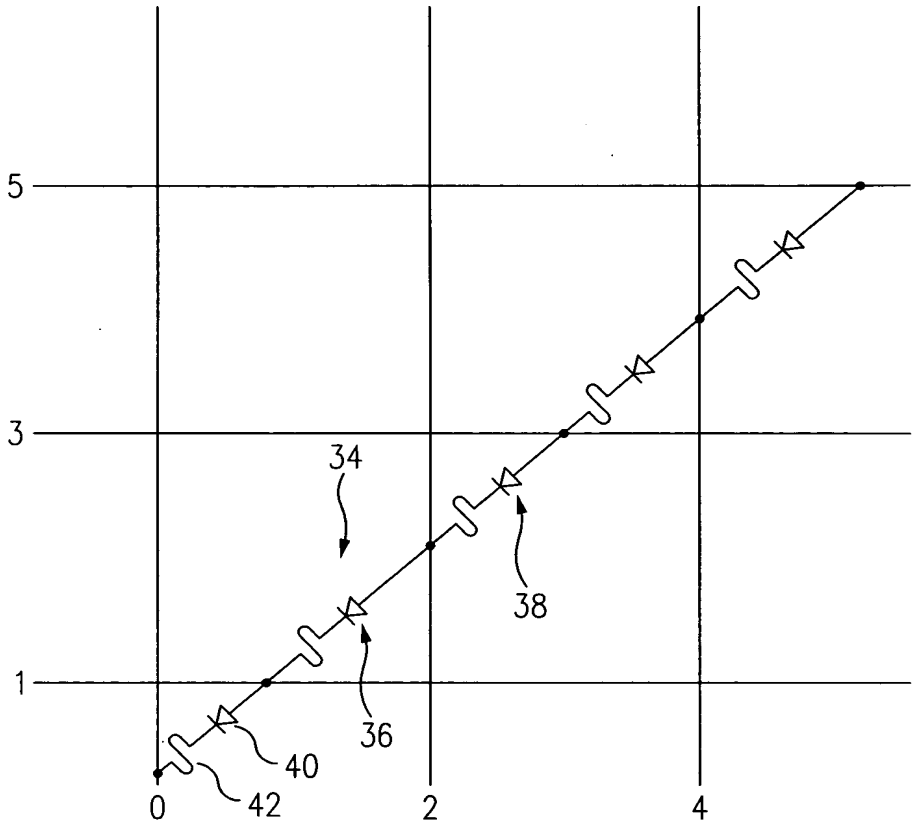

5
3
1
0
2
4
34
36
38
40
42

FIG. 3

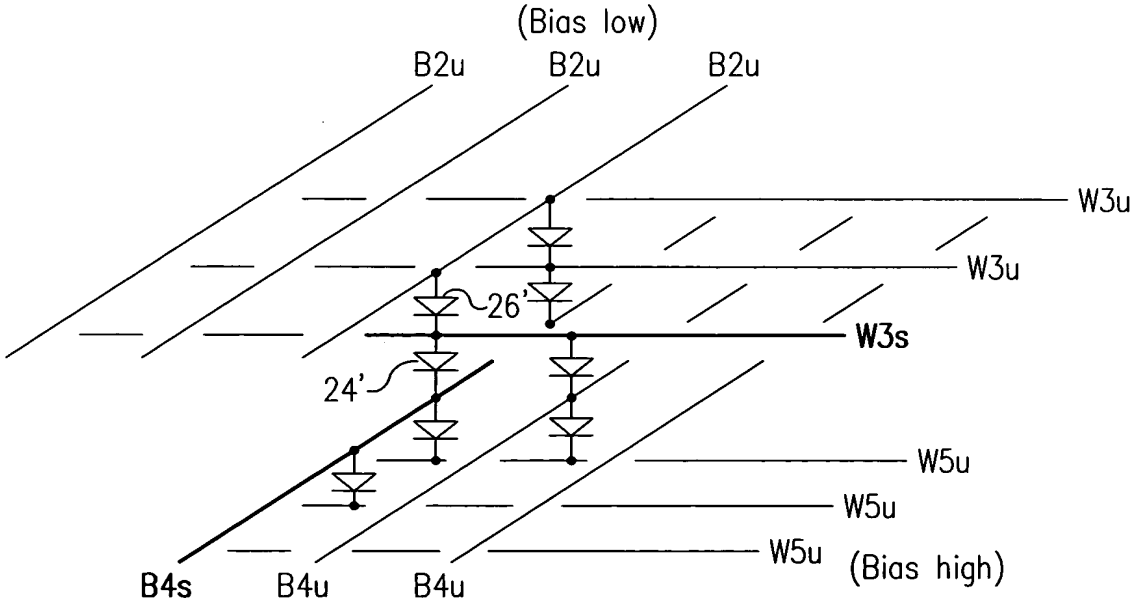

(Bias low)
B2u
B2u
B2u
W3u
W3u
26'
W3s
24'
W5u
W5u
W5u
(Bias high)
B4s
B4u
B4u

FIG. 4

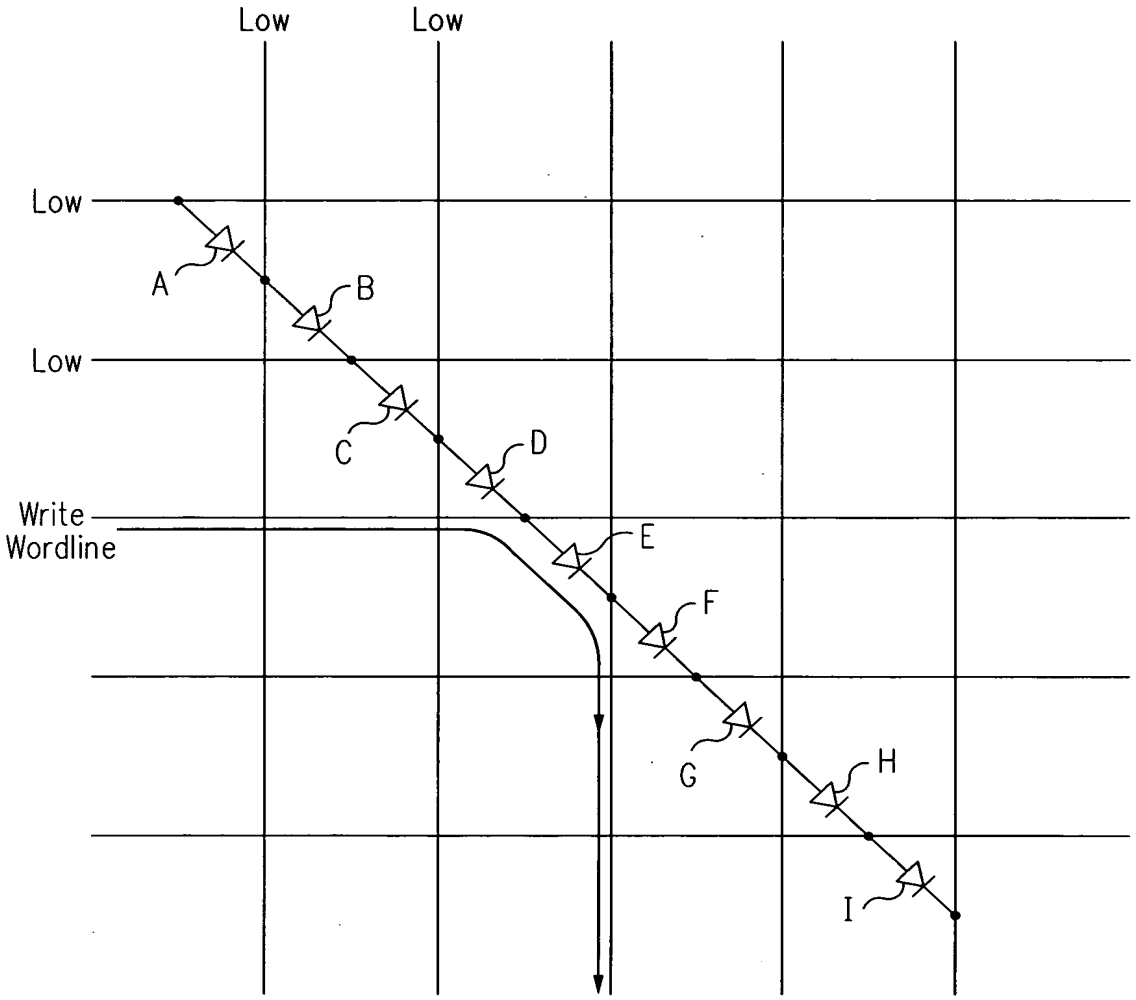



FIG. 5

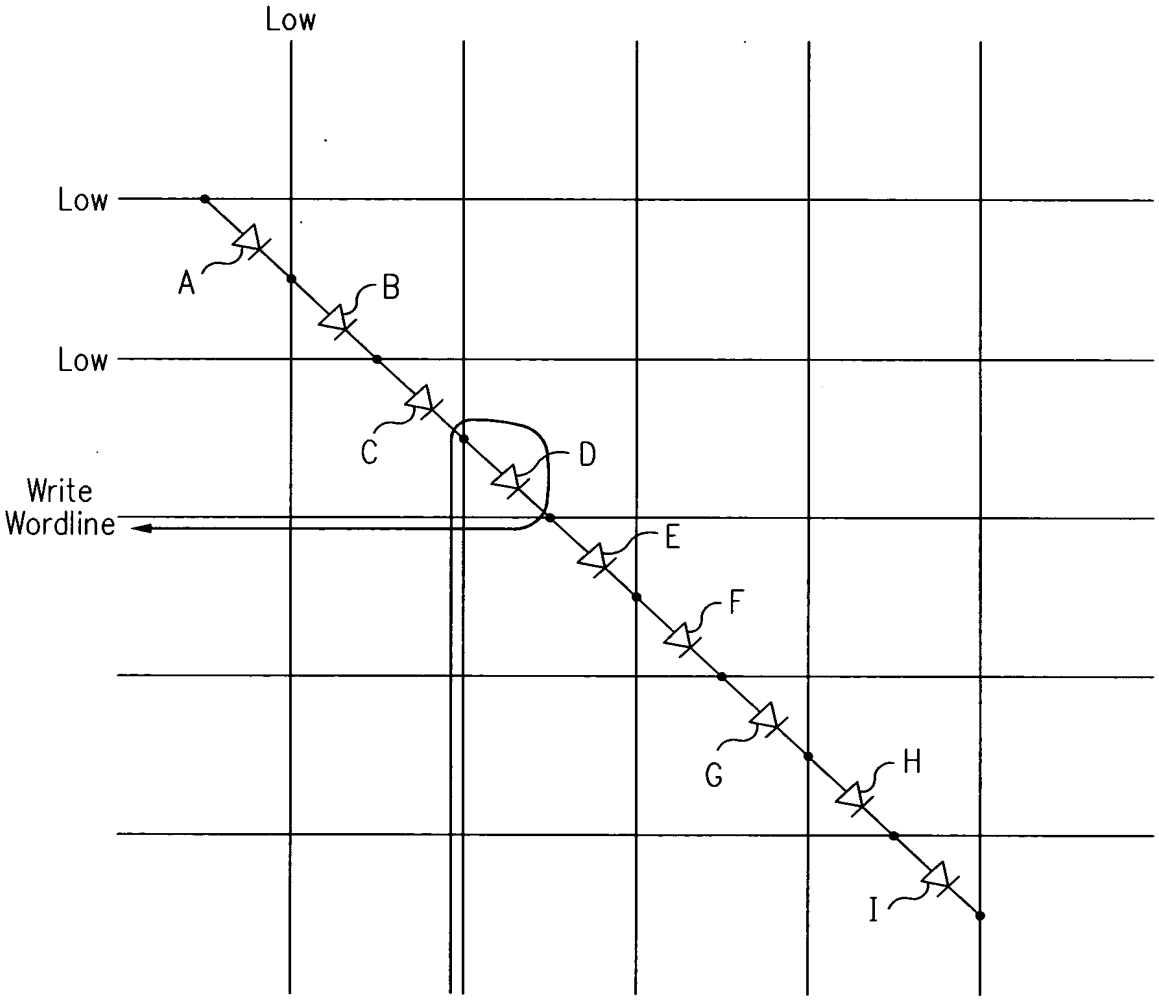



FIG. 6

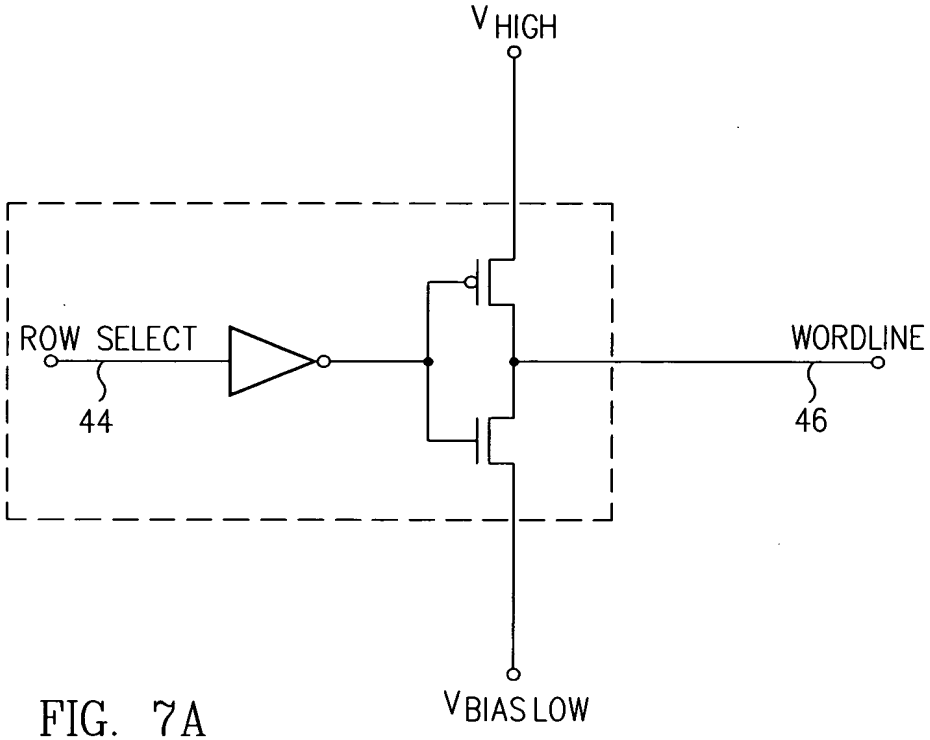

V HIGH
ROW SELECT
44
WORDLINE
46
V BIAS LOW

FIG. 7A

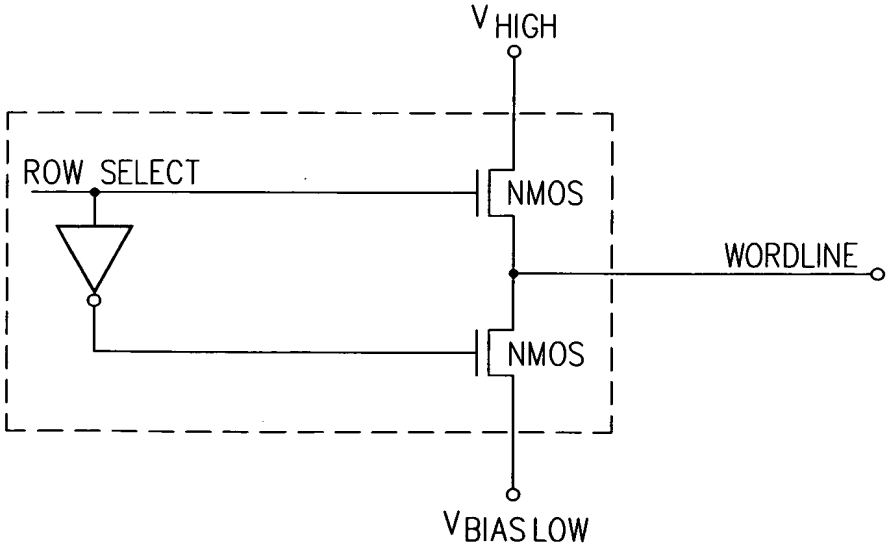

V HIGH
ROW SELECT
NMOS
WORDLINE
NMOS
V BIAS LOW

FIG. 7B

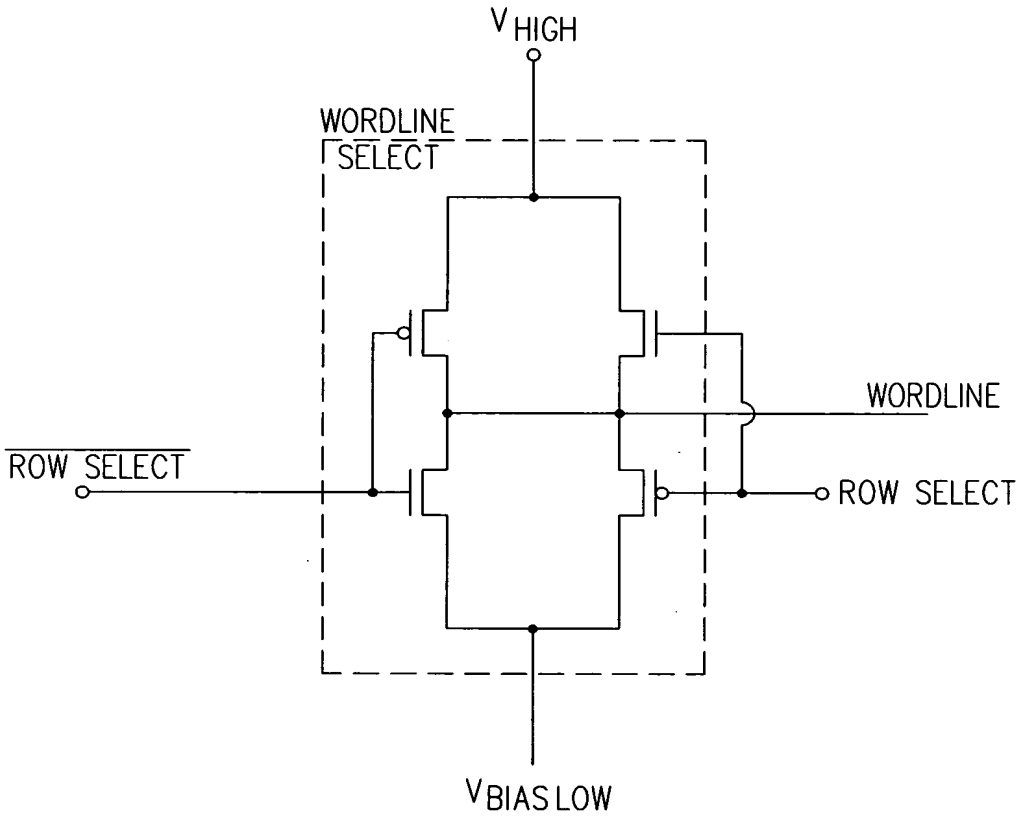
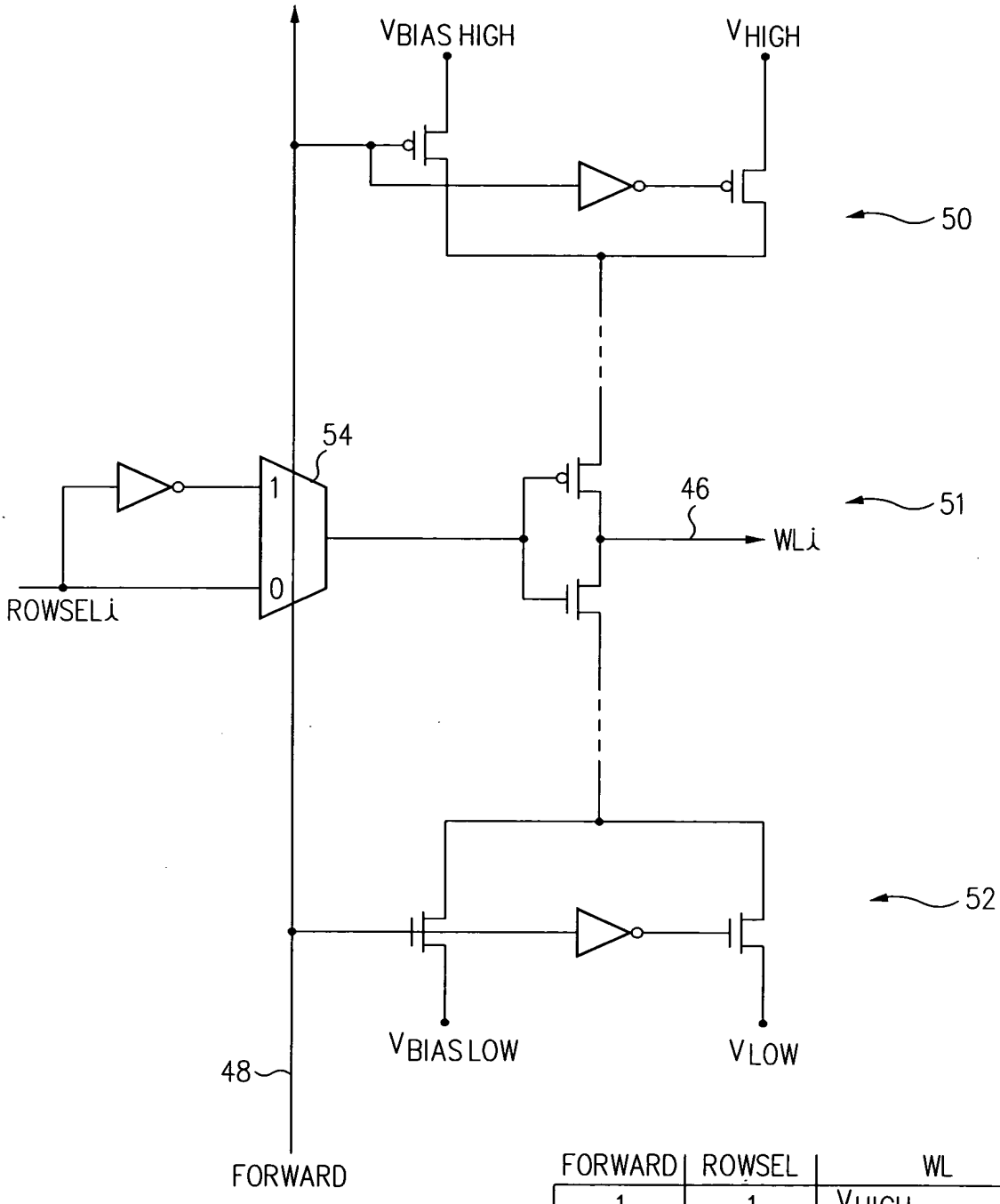

V HIGH
WORDLINE SELECT
WORDLINE
ROW SELECT
ROW SELECT
V BIAS LOW

FIG. 7C




| FORWARD | ROWSEL | WL |
|---|---|---|
| 1 | 1 | $V_{HIGH}$ |
| 1 | 0 | $V_{BIAS\ LOW}$ |
| 0 | 1 | $V_{LOW}$ (e.g. GND) |
| 0 | 0 | $V_{BIAS\ HIGH}$ |

FIG. 8

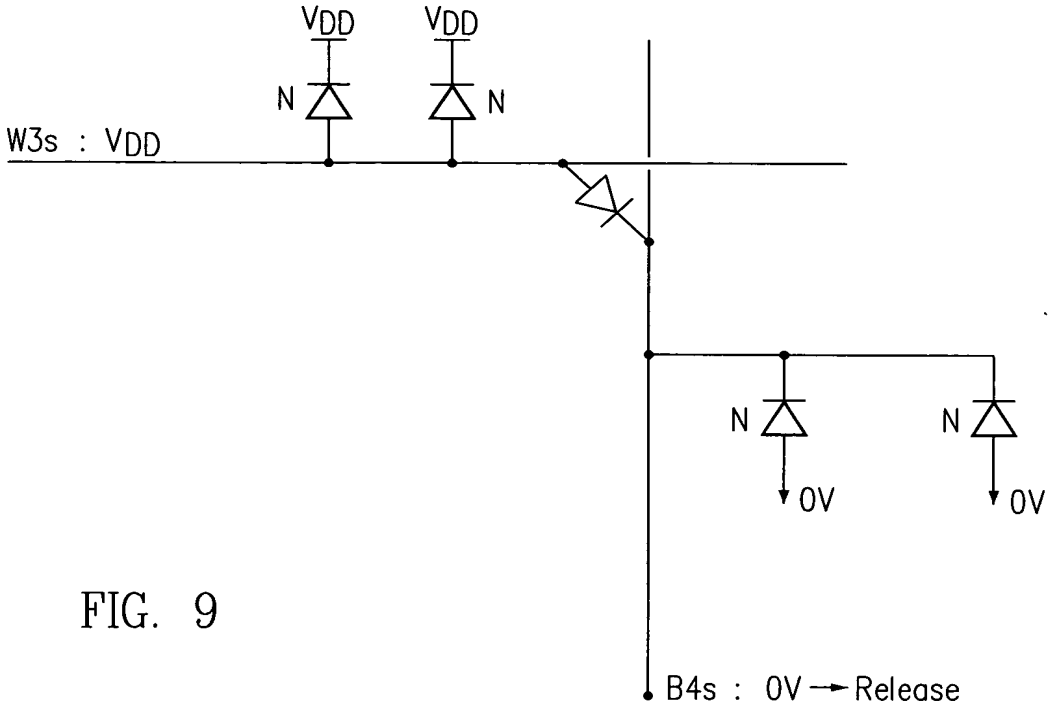

VDD
VDD
N
N
W3s : VDD
N
N
0V
0V
B4s : 0V → Release

FIG. 9

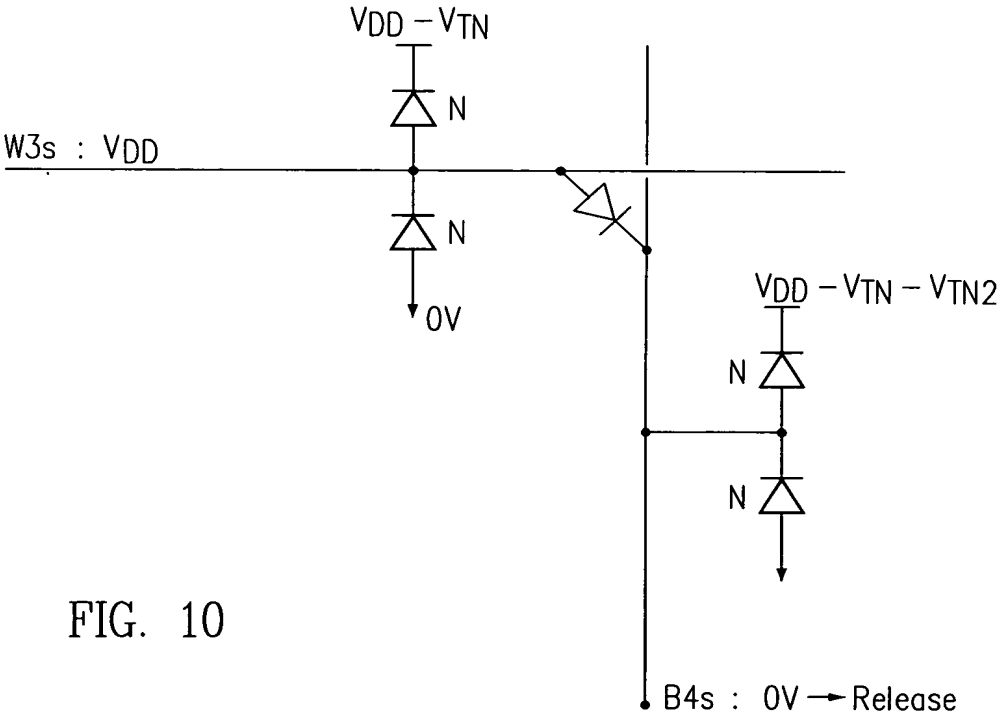

VDD – VTN
N
W3s : VDD
N
0V
VDD – VTN – VTN2
N
N
B4s : 0V → Release

FIG. 10

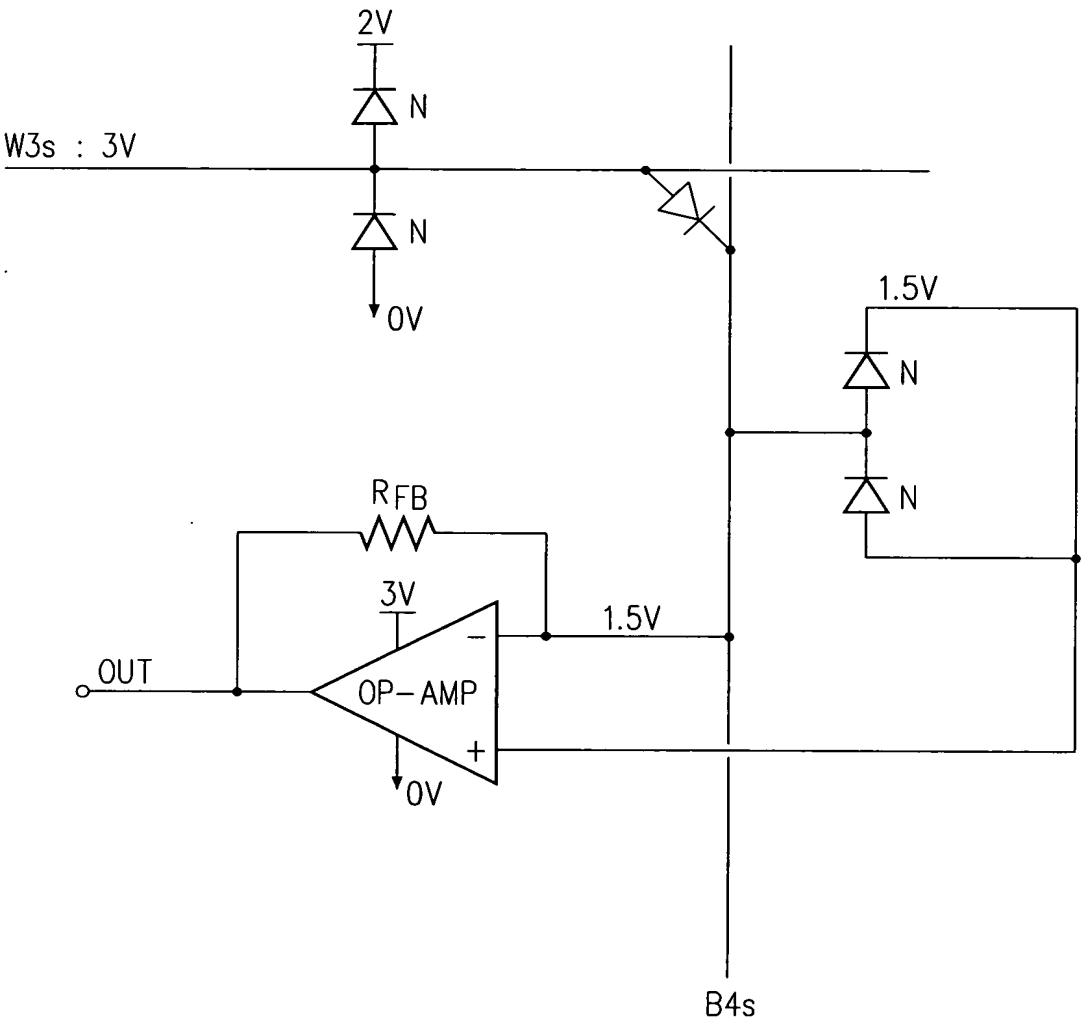



FIG. 11

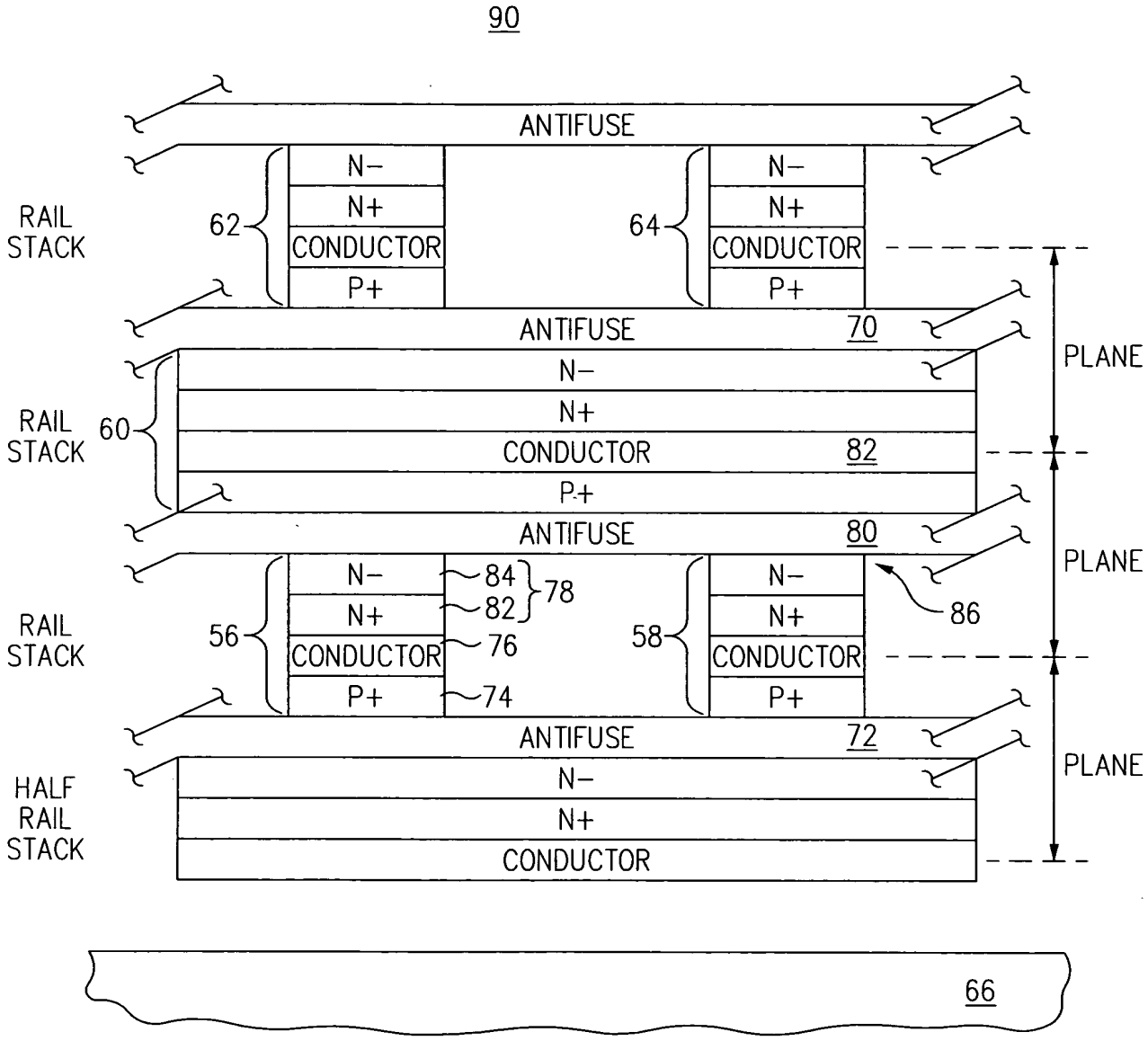

90
ANTIFUSE
N-
N+
CONDUCTOR
P+
62
64
RAIL STACK
ANTIFUSE
70
PLANE
60
82
80
56
58
84
82
78
76
74
86
72
HALF RAIL STACK
66

FIG. 12

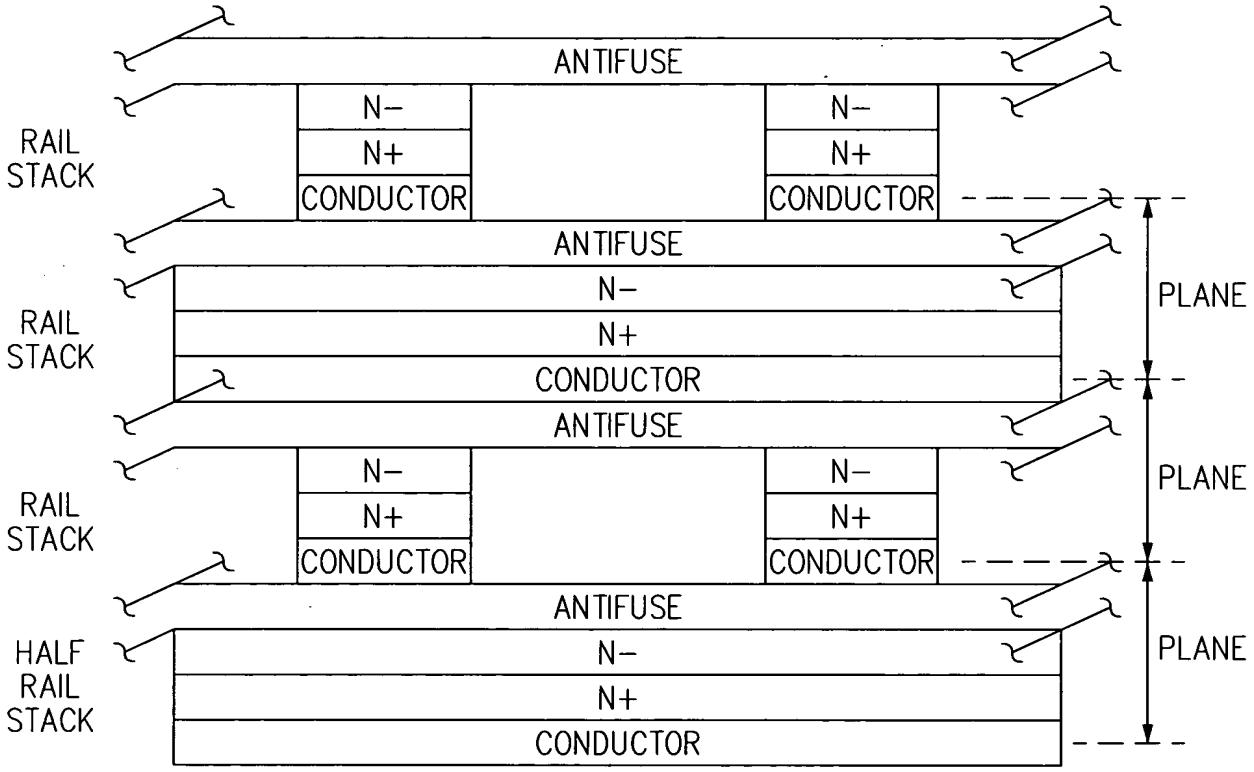

ANTIFUSE
N–
N+
CONDUCTOR
RAIL STACK
ANTIFUSE
N–
N+
CONDUCTOR
PLANE
RAIL STACK
ANTIFUSE
N–
N+
CONDUCTOR
PLANE
RAIL STACK
ANTIFUSE
N–
N+
CONDUCTOR
PLANE
HALF RAIL STACK

FIG. 13

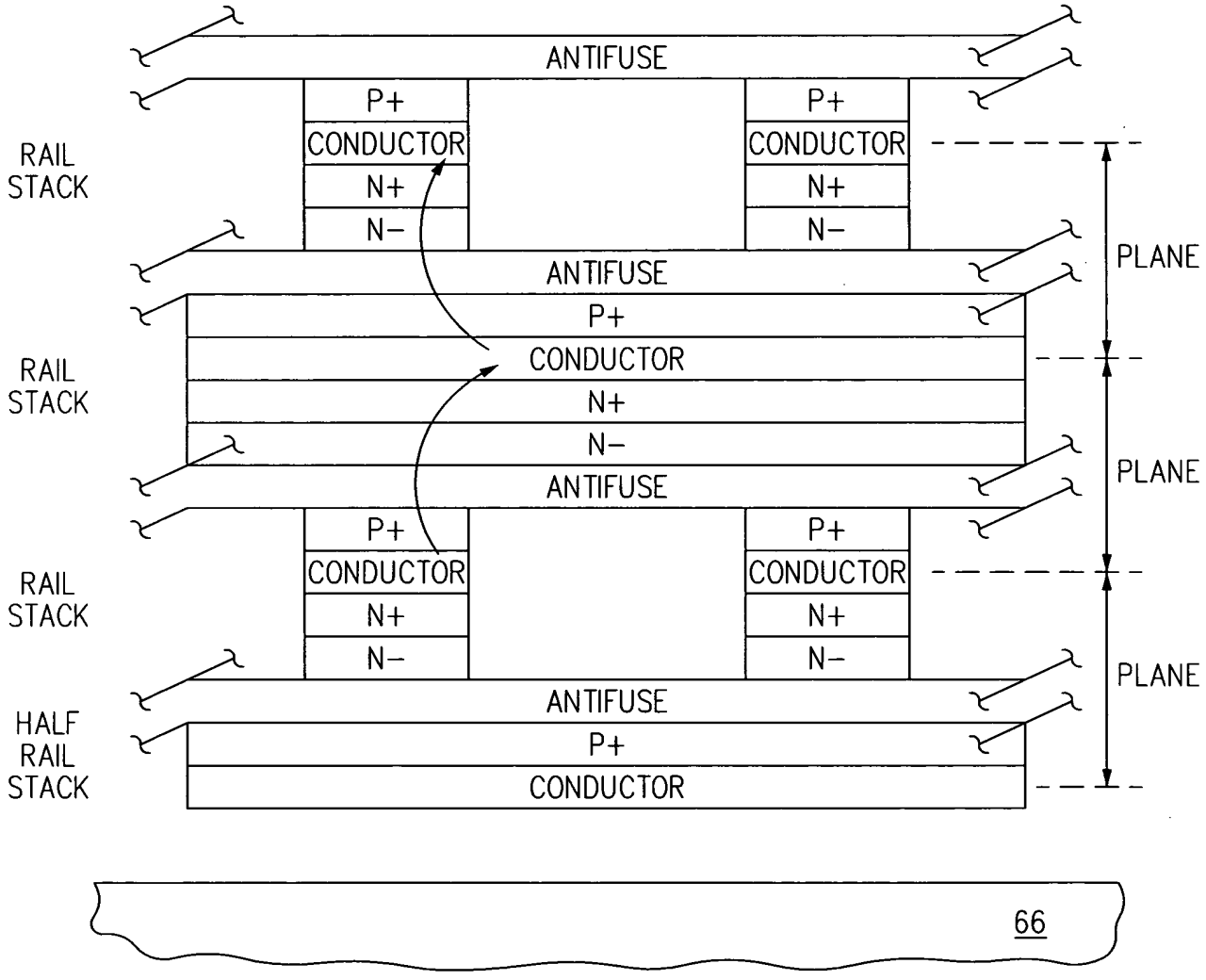



FIG. 14

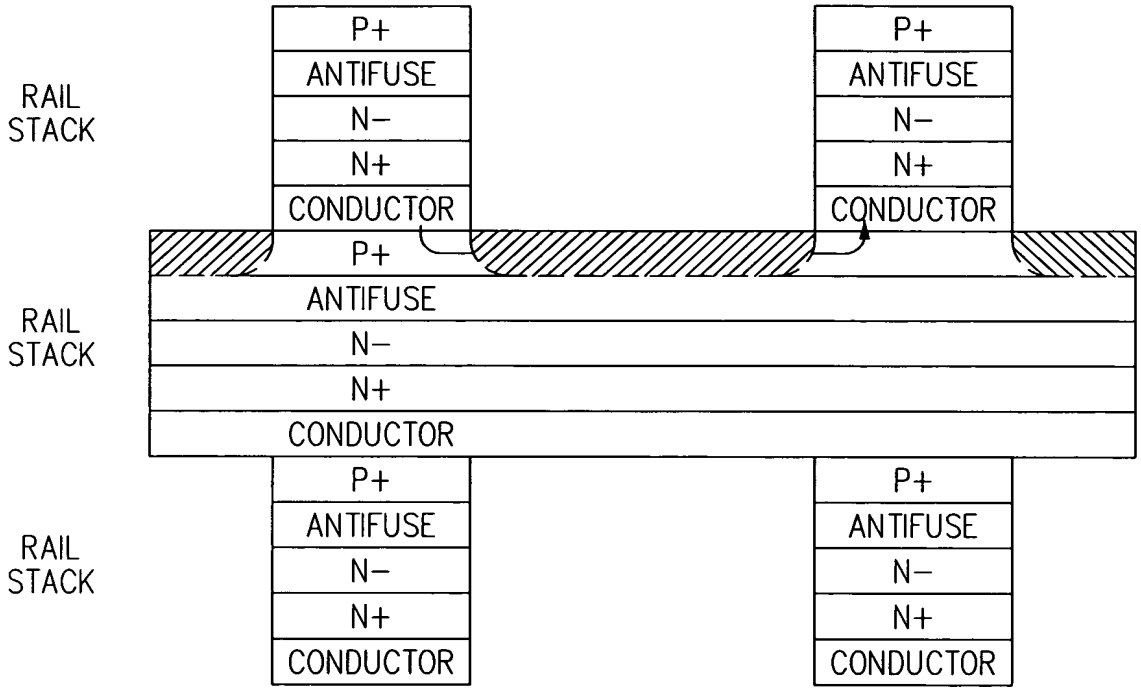

RAIL STACK
RAIL STACK
RAIL STACK
P+
ANTIFUSE
N–
N+
CONDUCTOR

FIG. 15

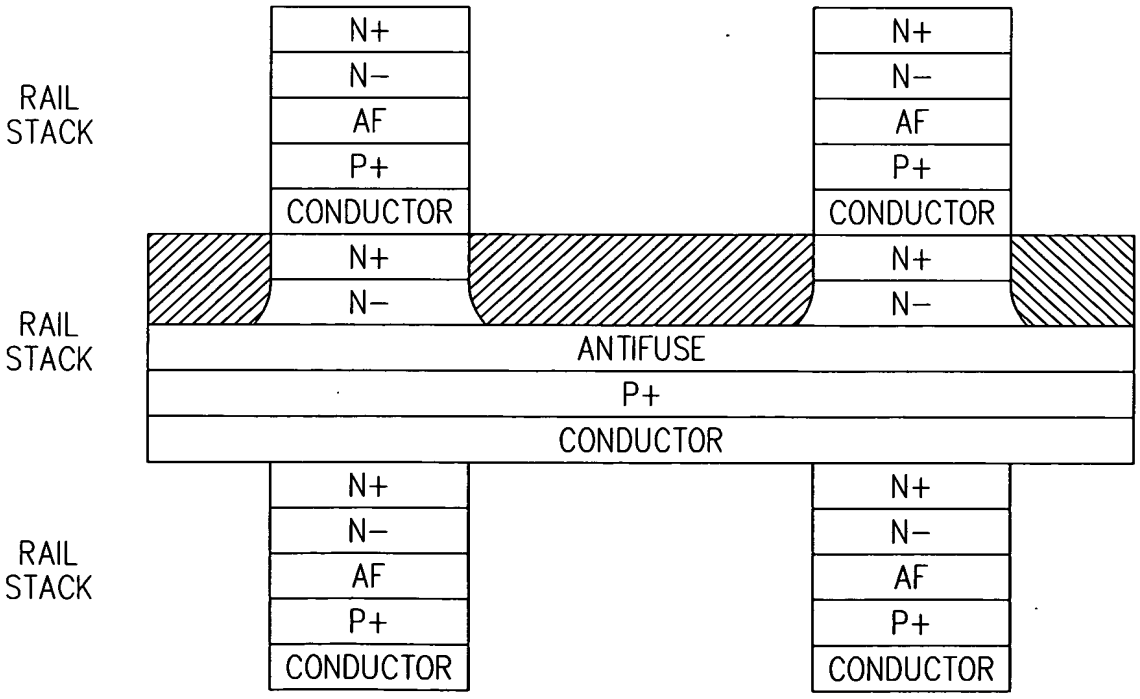

RAIL STACK
RAIL STACK
RAIL STACK
N+
N–
AF
P+
CONDUCTOR
ANTIFUSE

FIG. 16

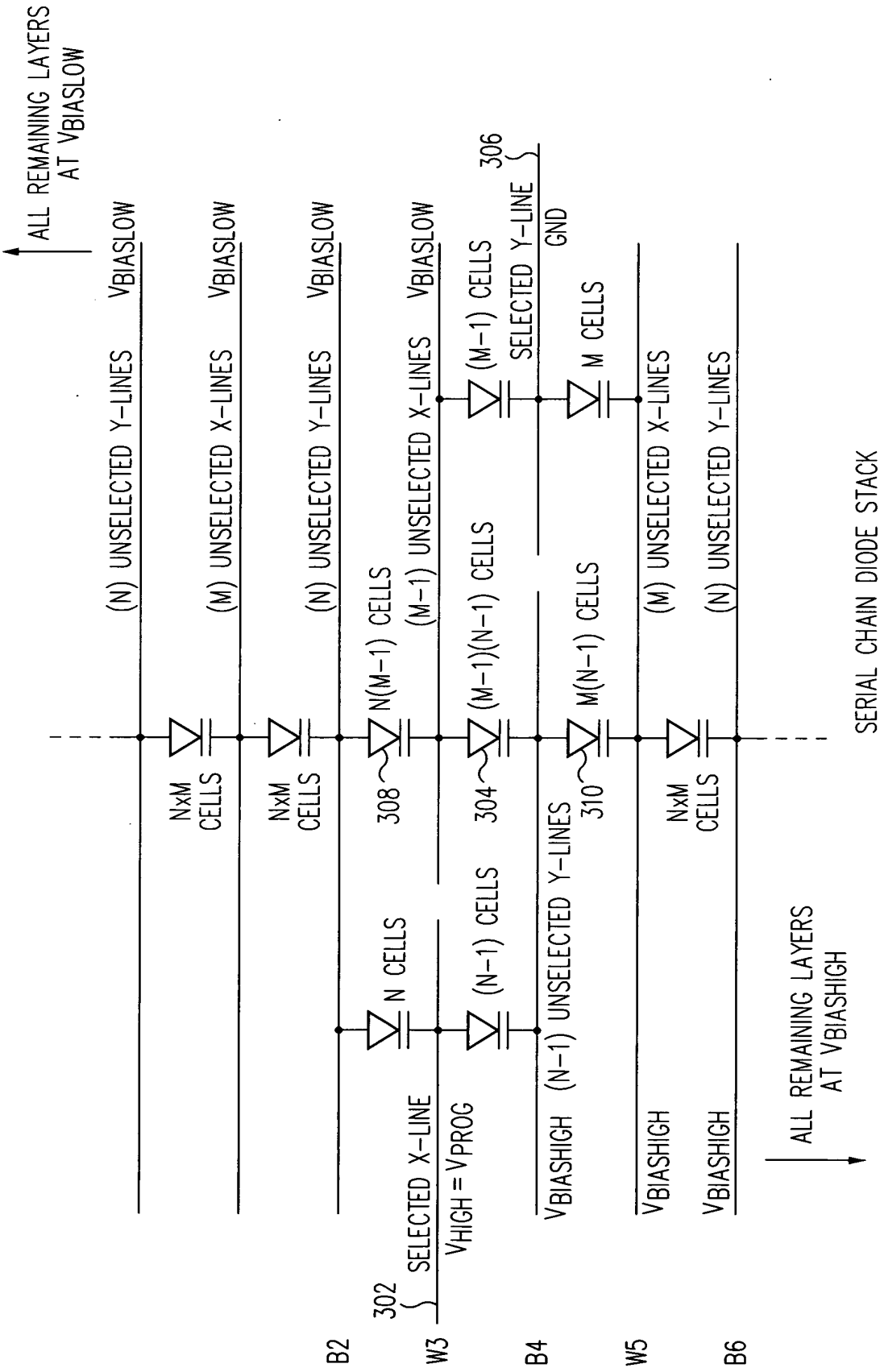

ALL REMAINING LAYERS AT VBIASLOW
(N) UNSELECTED Y-LINES VBIASLOW
(M) UNSELECTED X-LINES VBIASLOW
(N) UNSELECTED Y-LINES VBIASLOW
(M-1) UNSELECTED X-LINES VBIASLOW
SELECTED Y-LINE GND
306
NxM CELLS
NxM CELLS
308
N(M-1) CELLS
304
(M-1)(N-1) CELLS
(M-1) CELLS
M CELLS
310
M(N-1) CELLS
N CELLS
(N-1) CELLS
302
SELECTED X-LINE
VHIGH = VPROG
VBIASHIGH (N-1) UNSELECTED Y-LINES
VBIASHIGH
VBIASHIGH
NxM CELLS
(M) UNSELECTED X-LINES
(N) UNSELECTED Y-LINES
B2
W3
B4
W5
B6
SERIAL CHAIN DIODE STACK WRITE MODE BIASES
ALL REMAINING LAYERS AT VBIASHIGH

FIG. 17

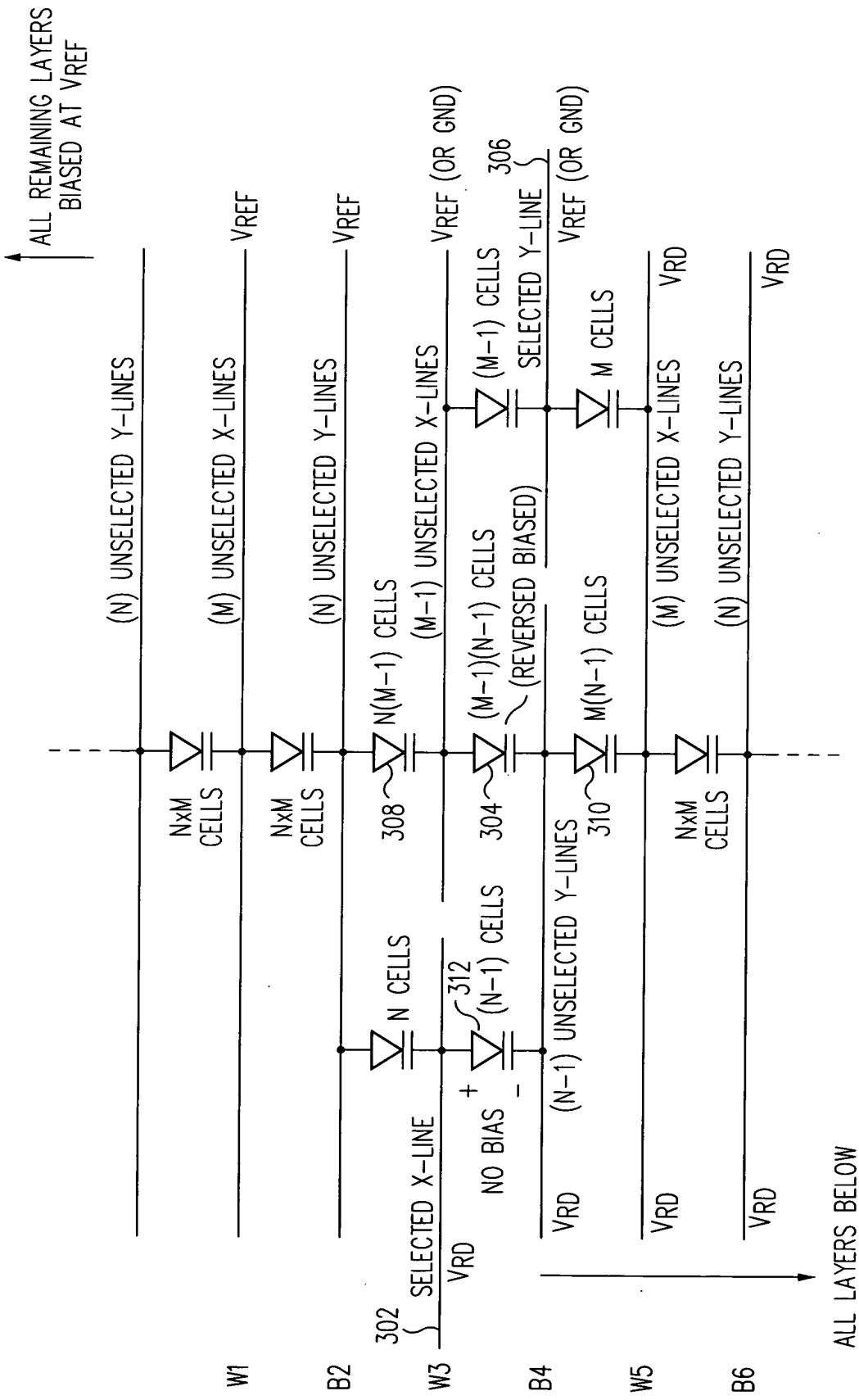

ALL REMAINING LAYERS BIASED AT VREF
(N) UNSELECTED Y-LINES
(M) UNSELECTED X-LINES
(N) UNSELECTED Y-LINES
(M-1) UNSELECTED X-LINES
(M-1) CELLS
SELECTED Y-LINE
M CELLS
(M) UNSELECTED X-LINES
(N) UNSELECTED Y-LINES
VREF
VREF
VREF (OR GND)
VREF (OR GND)
VRD
VRD
NxM CELLS
NxM CELLS
N(M-1) CELLS
(M-1)(N-1) CELLS
(REVERSED BIASED)
M(N-1) CELLS
NxM CELLS
308
304
310
306
N CELLS
(N-1) CELLS
312
(N-1) UNSELECTED Y-LINES
SELECTED X-LINE
NO BIAS
302
VRD
VRD
VRD
SERIAL CHAIN DIODE STACK
READ MODE BIASES
ALL LAYERS BELOW BIASED AT VRD
W1
B2
W3
B4
W5
B6

FIG. 18

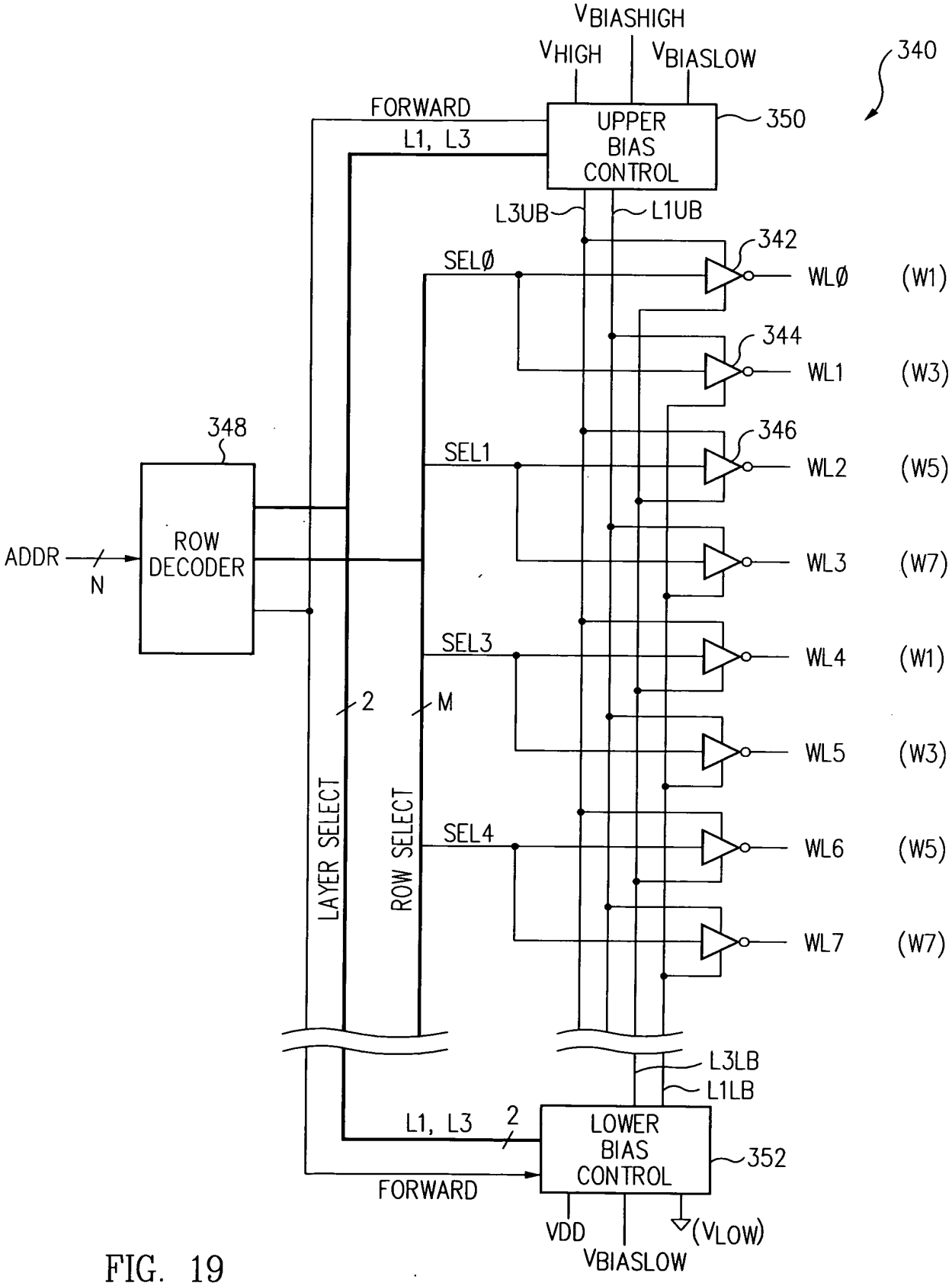
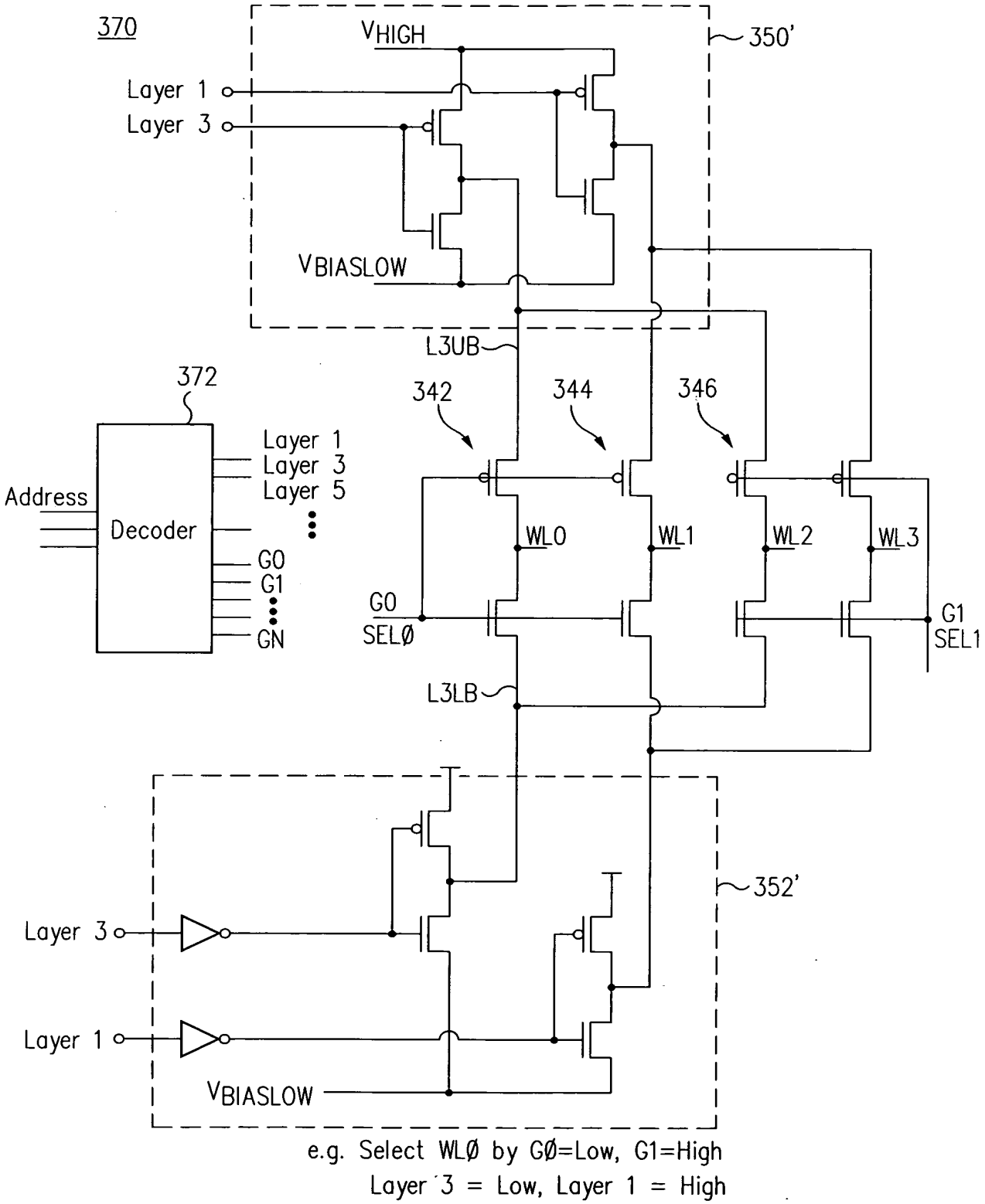

VBIASHIGH
VHIGH
VBIASLOW
340
FORWARD
L1, L3
UPPER BIAS CONTROL
350
L3UB
L1UB
342
SELØ
WLØ
(W1)
344
WL1
(W3)
348
346
SEL1
WL2
(W5)
ADDR
N
ROW DECODER
WL3
(W7)
SEL3
WL4
(W1)
2
M
WL5
(W3)
LAYER SELECT
ROW SELECT
SEL4
WL6
(W5)
WL7
(W7)
L3LB
L1LB
L1, L3
2
LOWER BIAS CONTROL
352
FORWARD
VDD
(VLOW)
VBIASLOW

FIG. 19




e.g. Select WLØ by GØ=Low, G1=High
Layer 3 = Low, Layer 1 = High

FIG. 20

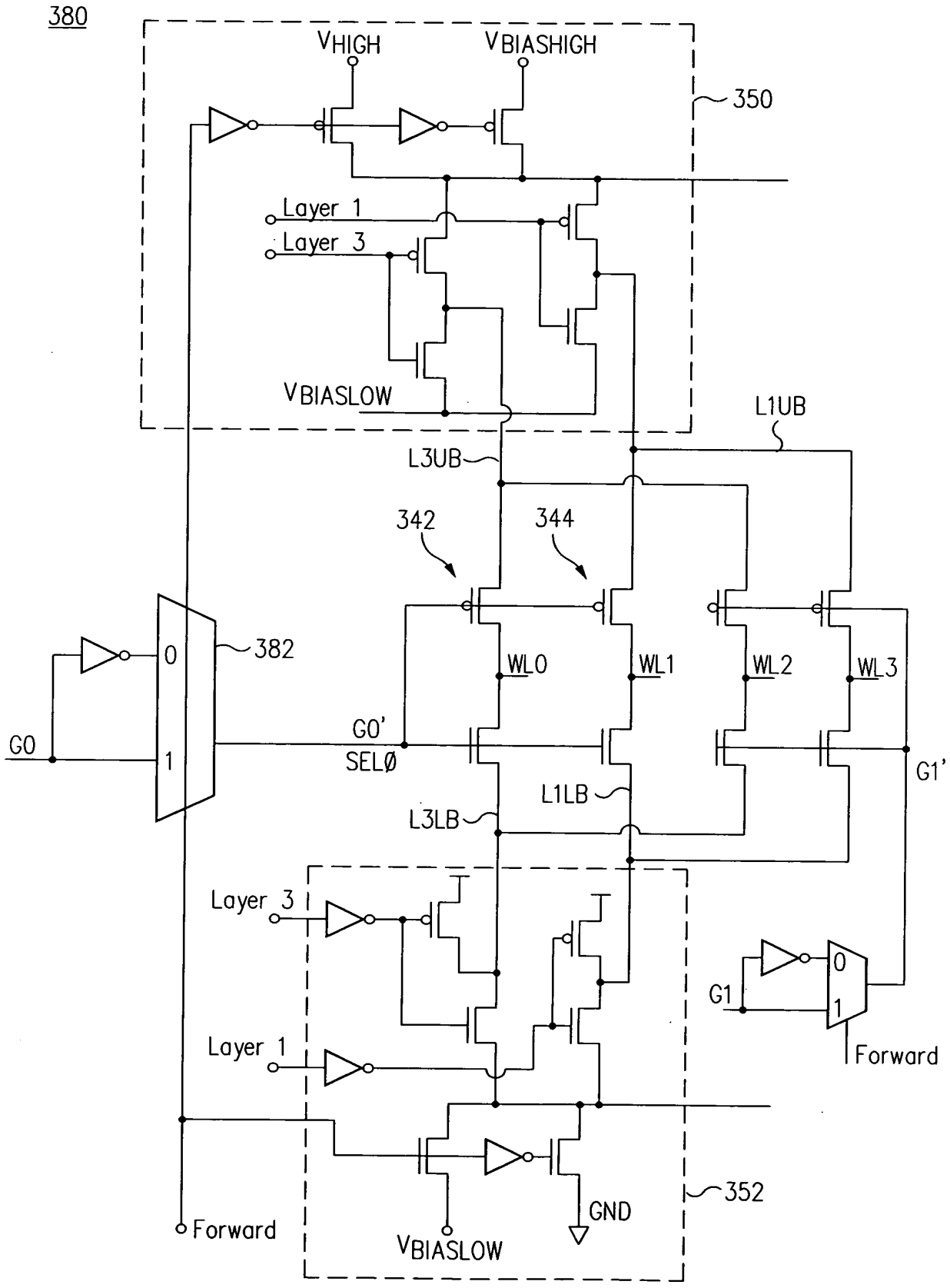

380
VHIGH
VBIASHIGH
350
Layer 1
Layer 3
VBIASLOW
L1UB
L3UB
342
344
382
0
1
G0
WL0
WL1
WL2
WL3
G0'
SELØ
L1LB
L3LB
G1'
Layer 3
Layer 1
G1
0
1
Forward
352
GND
Forward
VBIASLOW

FIG. 21

FIG. 22

| | | | $V_{HIGH} = V_{PROG}$<br>$V_{BIASLOW} = V_{UXL}$ | $V_{HIGH} = V_{RD}$<br>$V_{BIASLOW} = 0$ OR $V_{REF}$ |
|---|---|---|---|---|
| FORWARD | ROW SEL | WORDLINE | WRITE | READ |
| 1 | GND | SELECTED | $V_{HIGH} = V_{PROG}$ | $V_{HIGH} = V_{RD}$ |
| | $V_{ROW}$ | UNSELECTED | $V_{BIASLOW}$ | $V_{BIASLOW} = 0$ OR $V_{REF}$ |
| 0 | $V_{HIGH}$ | SELECTED | GND | GND |
| | GND | UNSELECTED | $V_{BIASLOW}$ | $V_{RD}$ |

SAME AS FOR BACK-TO-BACK DIODE STACK

$V_{PROG} \cong 9V$
$V_{RD} \cong 2V$
$V_{UXL} \cong 0.8V$

SERIAL CHAIN DIODE STACK
X-LINE BIAS VOLTAGES

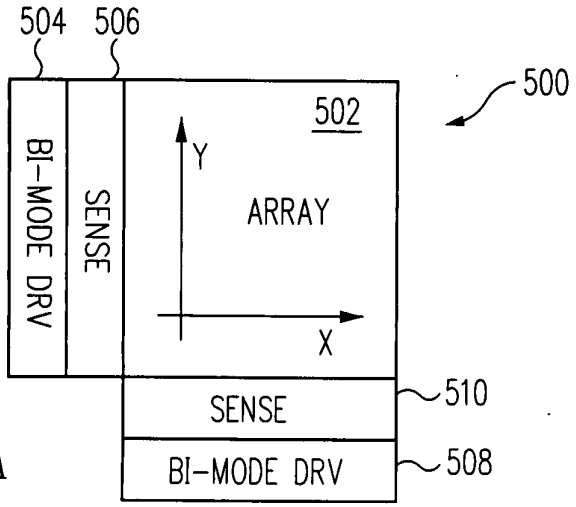



FIG. 23A

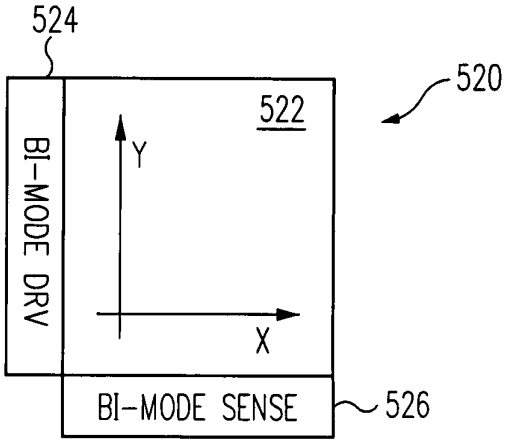



FIG. 23B